WE CLAIM:

1. A process for forming a conductive element, comprising:

providing a semiconductor substrate;

depositing a sacrificial material over the substrate;

forming an insulating layer over the sacrificial material;

forming an opening through the insulating layer to partially expose the sacrificial material;

selectively removing the sacrificial material to form a buried open volume; and

simultaneously depositing a conductor in the buried open volume and the opening to form the conductive element.

2. The process of Claim 1, wherein simultaneously depositing the conductor comprises performing atomic layer deposition.

3. The process of Claim 1, wherein simultaneously depositing the conductor comprises simultaneously completely filling the open volume and the opening with a conductor.

4. The process of Claim 1, further comprising depositing the sacrificial material into the opening, forming an additional insulating layer over the opening and forming an additional opening in the additional insulating layer before selectively removing the sacrificial material.

5. The process of Claim 4, further comprising depositing a barrier layer by atomic layer deposition after forming an additional opening and before simultaneously depositing the conductor.

6. The method of Claim 4, wherein the opening is a via and the additional opening is a trench.

7. The method of Claim 1, wherein the sacrificial material completely fills the open volume before being selectively removed.

8. The process of Claim 1, wherein the sacrificial material comprises a metal.

9. The process of Claim 8, wherein the metal comprises aluminum.

10. The process of Claim 9, wherein selectively removing the sacrificial material comprises etching the metal with chlorine gas.

11. The process of Claim 8, wherein the metal comprises nickel.

12. The process of Claim 11, wherein selectively removing the sacrificial material comprises etching the metal with carbon monoxide gas.

13. The process of Claim 1, wherein the sacrificial material comprises an organic material.

14. The process of Claim 13, wherein the organic material comprises a photoresist.

15. The process of Claim 14, wherein selectively removing the sacrificial material comprises stripping away the sacrificial material by wet ashing.

16. The process of Claim 15, wherein stripping away the sacrificial material by wet ashing comprises reacting the sacrificial material with a sulfuric acid and hydrogen peroxide solution.

17. The process of Claim 14, wherein selectively removing the sacrificial material comprises stripping away the sacrificial material by dry ashing.

18. The process of Claim 17, wherein stripping away the sacrificial material by dry ashing comprises reacting the sacrificial material with an ozone or an oxygen plasma.

19. The process of Claim 1, wherein the sacrificial material comprises a material that can be sublimed below about 400°C.

20. The process of Claim 19, wherein the material comprises antimony trioxide (Sb_2O_3) or tellurium (Te).

21. A method of semiconductor processing, comprising:

providing a partially fabricated integrated circuit having a top surface and a generally vertical opening leading to a buried open volume, wherein the buried open volume extends laterally beneath the top surface; and

forming a conductive line under the top surface by substantially filling the buried open volume with a conductor.

22. The method of Claim 21, wherein the buried open volume comprises a plurality of contiguous trenches and vias.

23. The method of Claim 21, wherein substantially filling the open volume comprises performing chemical fluid deposition, with the conductor dissolved in a supercritical fluid.

24. The method of Claim 23, wherein the supercritical fluid used in chemical fluid deposition is supercritical carbon dioxide and wherein the conductor is dissolved in the supercritical fluid at a temperature of about 60°C and a pressure of about 150 bar.

25. The method of Claim 21, wherein substantially filling the open volume comprises depositing the conductor by atomic layer deposition.

26. The method of Claim 21, wherein forming a conductive line comprises depositing a metal selected from the group comprising copper, silver and gold.

27. The method of Claim 21, wherein forming a conductive line comprises filling the open volume with a conductive polymer.

28. The method of Claim 27, wherein the conductive polymer is chosen from the group consisting of polyaniline, polypyrrole, polythiophenes and iodine doped polyacetylene.

29. The method of Claim 21, wherein forming a conductive line comprises forming a wire comprising carbon nanotube bits, wherein forming the wire comprises:

suspending the carbon nanotube bits in a supercritical fluid to form a carbon nanotube mixture;

introducing the mixture into the open volume;

removing the supercritical fluid by vaporization; and

applying a weak electric field to join the carbon nanotube bits together.

30. The method of Claim 21, wherein forming a conductive line comprises:

forming a nanometal slurry by suspending a nanometal powder in a supercritical fluid;

introducing the slurry into the open volume;

removing the supercritical fluid by decreasing a pressure of an ambient atmosphere of the partially fabricated integrated circuit;

subsequently sintering the nanometal powder by heating the partially fabricated integrated circuit to a temperature between about 200°C and about 300°C.

31. The method of Claim 30, wherein the nanometal powder consists of particles having a diameter of about 1-3 nm, particles having a diameter of about 5-8 nm and particles having a diameter of about 10-20 nm.

32. The method of Claim 21, wherein the conductor comprises polaron threads.

33. The method of Claim 21, wherein the partially fabricated integrated circuit comprises at least two wafers bonded together.

34. A method of semiconductor processing, comprising:

providing a semiconductor wafer having a sacrificial material, wherein the sacrificial material extends horizontally underneath a top surface of the wafer;

removing the sacrificial material to form an opening, wherein the opening spans more than one fabrication level; and

depositing at least one monolayer of a material within the opening.

35. The method of Claim 34, further comprising depositing a diffusion layer after removing the sacrificial material and before depositing at least one monolayer.

36. The method of Claim 35, wherein the diffusion layer is deposited by atomic layer deposition.

37. The method of Claim 35, wherein the diffusion layer comprises tungsten nitride carbide.

38. The method of Claim 35, wherein the at least one monolayer comprises copper, silver, gold or a polymer.

39. The method of Claim 34, wherein the material is conductive.

40. The method of Claim 39, wherein depositing at least one monolayer of a material comprises depositing monolayers until the opening is filled with the material.

41. The method of Claim 39, wherein depositing at least one monolayer of a material forms a conductive line for connecting electrical devices.

42. The method of Claim 34, wherein a cross-sectional area of the opening increases with decreasing distance to the top surface.

43. An integrated circuit comprising:

a generally horizontally extending buried conductive element;

a generally vertically extending conductive plug overlying and in contact with the buried conductive element; and

a generally horizontally extending conductive line overlying and in contact with the conductive plug,

wherein a first minimum dimension of the conductive element is smaller than a second minimum dimension of the conductive plug and the second minimum of the conductive plug is smaller than a third minimum dimension of the conductive line.

44. The integrated circuit of Claim 43, wherein the conductive element, the conductive plug and the conductive line forming an integral contiguous conductive path.

45. The integrated circuit of Claim 44, wherein the conductive element, the conductive plug and the conductive line comprise a material selected from the group consisting of copper, silver, gold and a polymer.

46. The integrated circuit of Claim 44, wherein the conductive element, the conductive plug and the conductive line are surrounded by a barrier layer.

47. The integrated circuit of Claim 46, wherein the barrier layer comprises a conductive material.

48. A semiconductor device, comprising:

a plurality of vertically spaced insulating layers;

at least two vertically spaced trenches provided in the insulating layers;

a contact via provided in one of the insulating layers, the contact via positioned between and forming a single continuous volume with the at least two trenches; and

a continuous barrier layer lining the at least two trenches and the contact via, wherein the barrier layer has a substantially uniform composition.

49. The semiconductor device of Claim 48, wherein the barrier layer has a substantially uniform thickness throughout the volume.

50. The semiconductor device of Claim 48, wherein the barrier layer comprises tungsten nitride carbide.

51. The semiconductor device of Claim 48, wherein the volume contains a conductor selected from the group consisting of copper, silver, gold and a polymer.

52. The semiconductor device of Claim 51, wherein the barrier layer surrounds the conductor to intervene between the conductor and the insulating layers.

53. The semiconductor device of Claim 52, wherein the barrier layer is conductive.

54. The semiconductor device of Claim 48, wherein a dielectric barrier layer does not intervene between the at least two insulating layers.